WHAT IS CLAIMED IS:

1. A memory controller comprising:

a CPU interface arranged to interface with a CPU;

a memory interface arranged to interface with a memory storing programs to be processed in the CPU and display data to be displayed on a display;

a display control circuit to control output of display data to the display;

a rendering process circuit to access the memory; and

a memory control circuit to control access to the memory from one of the CPU, the display controller and the rendering processor,

wherein, when an access to the memory from the CPU is requested at the time when the rendering process circuit accesses the memory, the memory control circuit stops the access to the memory from the rendering process circuit until the access to the memory from the CPU ends, and when the access to the memory from the CPU ends, resumes the access to the memory from the rendering process circuit from the beginning.

2. A memory controller according to claim 1, wherein the memory control circuit is connected to the CPU, via a CPU bus, and to the memory, via a memory bus, for providing priority to the access from the CPU to the memory.

3. A memory controller according to claim 2, wherein the memory control circuit comprises:

a first decoder to generate a CPU bus access request signal, when an access request is issued from the CPU;

a second decoder to generate an internal bus access start signal when an access request is issued from an internal bus;

a CPU access buffer to receive the CPU bus access request signal, and to produce a CPU bus access valid signal which exhibits a high logic state during execution of the memory access from the CPU, and returns to a low logic state after the memory access from the CPU ends;

a CPU bus access length calculation circuit to calculate the number of cycles required for the memory access from the CPU, and to produce a CPU access length;

an internal bus access counter, reset upon receipt of the internal bus access start signal, to count the number of cycles during execution of an internal bus access and to produce an internal access cycle;

a stop decision circuit to generate a switching start cycle indicating the timing for setting a switching signal, and a stop start cycle indicating the timing for setting a stop signal;

a switching signal generation circuit to generate the switching signal for controlling the memory access from one of the CPU and the rendering process circuit, on the basis of the CPU access length, the internal access cycle, and the switching start cycle; and

a stop processing circuit to generate the stop signal for stopping the memory access from the rendering process circuit until the end of the memory access from the CPU, on the basis of a command outputted from the second decoder, the CPU access length output from the CPU bus access length calculation circuit, and the internal bus access outputted from the internal bus access counter, and the stop start cycle.

4. A memory controller according to claim 3, wherein the stop decision circuit comprises:

a transfer time register to register a transfer time of a command from the CPU bus to the memory bus, when an access is issued from the CPU;

a memory characteristic register to register read and write pre-charge latencies;

a read stop decision circuit to generate the switching start cycle indicating the timing for setting the switching signal during execution of a read access and the stop start cycle indicating the timing for setting the stop signal on the basis of the stop request cycle, the internal access length, the transfer time and the read pre-charge latency; and

a write stop decision circuit to generate the switching start cycle indicating the timing for setting the switching signal during execution of a write access and the stop start cycle indicating the timing for setting the stop signal on the basis of the stop request cycle, the internal access length, the transfer time and the write pre-charge latency.

5. A memory controller according to claim 4, wherein the read stop decision circuit comprises:

a comparator to compare the internal access length and the stop request cycle;

an adder to add the stop request cycle and the transfer time, and to output the switching start cycle from the stop request cycle and the transfer time; and

a substractor to subtract the read pre-charge latency from the switching start cycle and to output a difference; and

a selector to select the output of the subtractor as a stop start cycle when the output of the comparator indicates a high logic state.

6. A memory controller according to claim 4, wherein the stop processing circuit comprises:

a memory characteristic register to register read and write pre-charge latencies;

a first comparator to compare the internal access cycle and the stop start cycle;

an adder to add the stop start cycle, the CPU access length, and a selected one of the read and write pre-charge latencies;

a second comparator to compare the output of the adder and the output of the first comparator; and

a stop register, set when the output of the first comparator indicates a high logic state, and reset when the output of the second comparator indicates a high logic state, to produce the stop signal.

7. A main controller IC chip comprising:

a CPU; and

a memory controller for controlling access of a memory, the memory controller comprising:

a CPU interface arranged to interface with a CPU;

a memory interface arranged to interface with the memory storing programs to be processed in the CPU and display data to be displayed on a display;

a display control circuit to control output of display data to the display;

a rendering process circuit to access the memory; and

a memory control circuit to control access to the memory from one of the CPU, the display control circuit and the rendering process circuit,

wherein, when an access to the memory from the CPU is requested at the time when the rendering process circuit accesses the memory, the memory control circuit stops the access to the memory from the rendering process circuit until the access to the memory from the CPU ends, and when the access to the memory from the CPU ends, resumes the access to the memory from the rendering process circuit from the beginning.

8. A main controller IC chip according to claim 7, wherein the memory control circuit is connected to the CPU, via a CPU bus, and to the memory, via a memory bus, for providing priority to the access from the CPU to the memory.

9. A main controller IC chip according to claim 8, wherein the memory control circuit comprises:

a first decoder to generate a CPU bus access request signal, when an access request is issued from the CPU;

a second decoder to generate an internal bus access start signal when an access request is issued from an internal bus;

a CPU access buffer to receive the CPU bus access request signal, and to produce a CPU bus access valid signal which exhibits a high logic state during execution of the memory access from the CPU, and returns to a low logic state after the memory access from the CPU ends;

a CPU bus access length calculation circuit to calculate the number of cycles required for the memory access from the CPU, and to produce a CPU access length;

an internal bus access counter, reset upon receipt of the internal bus access start signal, to count the number of cycles during execution of an internal bus access and to produce an internal access cycle;

a stop decision circuit to generate a switching start cycle indicating the timing for setting a switching signal, and a stop start cycle indicating the timing for setting a stop signal;

a switching signal generation circuit to generate the switching signal for controlling the memory access from one of the CPU and the rendering process circuit, on the basis of the CPU access length, the internal access cycle, and the switching start cycle; and

a stop processing circuit to generate the stop signal for stopping the memory access from the rendering process circuit until the end of the memory access from the CPU, on the basis of a command outputted from the second decoder, the CPU access length output from the CPU bus access length calculation circuit, and the internal bus access outputted from the internal bus access counter, and the stop start cycle.

10. A main controller IC chip according to claim 9, wherein the stop decision circuit comprises:

a transfer time register to register a transfer time of a command from the CPU bus to the memory bus, when an access is issued from the CPU;

a memory characteristic register to register read and write pre-charge latencies;

a read stop decision circuit to generate the switching start cycle indicating the timing for setting the switching signal during execution of a read access and the stop start cycle indicating the timing for setting the stop signal on the basis of the stop request cycle, the internal access length, the transfer time and the read pre-charge latency; and

a write stop decision circuit to generate the switching start cycle indicating the timing for setting the switching signal during execution of a write access and the stop start cycle indicating the timing for setting the stop signal on the basis of the stop request cycle, the internal access length, the transfer time and the write pre-charge latency.

11. A main controller IC chip according to claim 10, wherein the read stop decision circuit comprises:

a comparator to compare the internal access length and the stop request cycle;

an adder to add the stop request cycle and the transfer time, and to output the switching start cycle from the stop request cycle and the transfer time; and

a substractor to subtract the read pre-charge latency from the switching start cycle and to output a difference; and

a selector to select the output of the subtractor as a stop start cycle when the output of the comparator indicates a high logic state.

12. A main controller IC chip according to claim 11, wherein the stop processing circuit comprises:

a memory characteristic register to register read and write pre-charge latencies;

a first comparator to compare the internal access cycle and the stop start cycle;

an adder to add the stop start cycle, the CPU access length, and a selected one of the read and write pre-charge latencies;

a second comparator to compare the output of the adder and the output of the first comparator; and

a stop register, set when the output of the first comparator indicates a high logic state, and reset when the output of the second comparator indicates a high logic state, to produce the stop signal.

13. A main controller IC chip comprising:

a CPU;

a memory to store programs to be processed in the CPU and display data to be displayed on a display;

a memory controller for controlling access of the memory, the memory controller comprising:

a CPU interface arranged to interface with a CPU;

a memory interface arranged to interface with the memory storing programs to be processed in the CPU and display data to be displayed on a display;

a display control circuit to control output of display data to the display;

a rendering process circuit to access the memory; and

a memory control circuit to control access to the memory from one of the CPU, the display control circuit and the rendering process circuit,

wherein, when an access to the memory from the CPU is requested at the time when the rendering process circuit accesses the memory, the memory control circuit stops the access to the memory from the rendering process circuit until the access to the memory from the CPU ends, and when the access to the memory from the CPU ends, resumes the access to the memory from the rendering process circuit from the beginning.

14. A main controller IC chip according to claim 13, wherein the memory control circuit is connected to the CPU, via a CPU bus, and to the memory, via a memory bus, for providing priority to the access from the CPU to the memory.

15. A main controller IC chip according to claim 14, wherein the memory control circuit comprises:

a first decoder to generate a CPU bus access request signal, when an access request is issued from the CPU;

a second decoder to generate an internal bus access start signal when an access request is issued from an internal bus;

a CPU access buffer to receive the CPU bus access request signal, and to produce a CPU bus access valid signal which exhibits a high logic state during execution of the memory access from the CPU, and returns to a low logic state after the memory access from the CPU ends;

a CPU bus access length calculation circuit to calculate the number of cycles required for the memory access from the CPU, and to produce a CPU access length;

an internal bus access counter, reset upon receipt of the internal bus access start signal, to count the number of cycles during execution of an internal bus access and to produce an internal access cycle;

a stop decision circuit to generate a switching start cycle indicating the timing for setting a switching signal, and a stop start cycle indicating the timing for setting a stop signal;

a switching signal generation circuit to generate the switching signal for controlling the memory access from one of the CPU and the rendering process circuit, on the basis of the CPU access length, the internal access cycle, and the switching start cycle; and

a stop processing circuit to generate the stop signal for stopping the memory access from the rendering process circuit until the end of the memory access from the CPU, on the basis of a command outputted from the second decoder, the CPU access length output from the CPU bus access length calculation circuit, and the

internal bus access outputted from the internal bus access counter, and the stop start cycle.

16. A main controller IC chip according to claim 15, wherein the stop decision circuit comprises:

a transfer time register to register a transfer time of a command from the CPU bus to the memory bus, when an access is issued from the CPU;

a memory characteristic register to register read and write pre-charge latencies;

a read stop decision circuit to generate the switching start cycle indicating the timing for setting the switching signal during execution of a read access and the stop start cycle indicating the timing for setting the stop signal on the basis of the stop request cycle, the internal access length, the transfer time and the read pre-charge latency; and

a write stop decision circuit to generate the switching start cycle indicating the timing for setting the switching signal during execution of a write access and the stop start cycle indicating the timing for setting the stop signal on the basis of the stop request cycle, the internal access length, the transfer time and the write pre-charge latency.

17. A main controller IC chip according to claim 15, wherein the read stop decision circuit comprises:

a comparator to compare the internal access length and the stop request cycle;

an adder to add the stop request cycle and the transfer time, and to output the switching start cycle from the stop request cycle and the transfer time; and

a substractor to subtract the read pre-charge latency from the switching start cycle and to output a difference; and

a selector to select the output of the subtractor as a stop start cycle when the output of the comparator indicates a high logic state.

18. A main controller IC chip according to claim 15, wherein the stop processing circuit comprises:

a memory characteristic register to register read and write pre-charge latencies;

a first comparator to compare the internal access cycle and the stop start cycle;

an adder to add the stop start cycle, the CPU access length, and a selected one of the read and write pre-charge latencies;

a second comparator to compare the output of the adder and the output of the first comparator; and

a stop register, set when the output of the first comparator indicates a high logic state, and reset when the output of the second comparator indicates a high logic state, to produce the stop signal.